AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph at page 66, line 20 to line 27, as follows:

The semiconductor thin films were formed by successively forming the following compound semiconductor layers on the GaAs substrate [[1]] two inches in diameter by the molecular beam epitaxy (MBE): 500 nm $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ as the first compound semiconductor layer; 50 nm InAs as the active layer; 50 nm $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ as the second compound semiconductor layer; and 5 nm $GaAs_{0.02}Sb_{0.98}$ as the third compound semiconductor layer.

Please amend the paragraph at page 67, line 1 to line 7, as follows:

The band gap of $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ is about 1.2 eV, which is sufficiently greater than 0.36 eV of InAs. The electric characteristics of the semiconductor thin film [[2]] were measured using the van der Pauw method. The results were: the electron mobility was 22000 cm^2/Vs, the sheet resistance was 360 Ω, and the sheet electron concentration was 7.9×10^{11} cm^{-2}.

Please amend the paragraph at page 69, line 19, to page 70, line 3, as follows:

Subsequently, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[3]] was formed by the common lift off method. After that, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the passivation [[4]] using plasma CVD. On the Si_3N_4 layer, a resist pattern was formed having openings at the pad portions. Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2. After removing the resist, the wafer was subjected to

250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 70, line 24, to page 71, line 4, as follows:

The semiconductor thin films were formed by successively forming the following compound semiconductor layers on the GaAs substrate [[1]] two inches in diameter by the molecular beam epitaxy (MBE): 500 nm $Al_{0.50}Ga_{0.50}As$ as the first compound semiconductor layer; 50 nm $In_{0.05}Ga_{0.95}As$ as the active layer; 50 nm $Al_{0.50}Ga_{0.50}As$ as the second compound semiconductor layer; and 10 nm GaAs as the third compound semiconductor layer.

Please amend the paragraph at page 71, line 23, to page 72, line 7, as follows:

Subsequently, a resist pattern with a shape of the magneto-sensitive pattern was formed. Using it as a mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate by ion milling, followed by removing the resist. Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the passivation [[4]] using plasma CVD. On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the $In_{0.05}Ga_{0.95}As$ layer and at the pad portions. Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2.

Please amend the paragraph at page 72, line 8 to line 15, as follows:

Subsequently, the resist was removed, followed by continuous evaporation of the 250 nm AuGe layer, 50 nm Ni layer and 350 nm Au layer by the vacuum evaporation method, and the pattern of the metal electrode layer [[3]] was formed by the common lift

off method. Finally, the wafer was subjected to 400°C, five minute annealing in an N_2 atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 73, line 22, to page 74, line 6, as follows:

Subsequently, continuous evaporation of the 250 nm AuGe layer, 50 nm Ni layer and 350 nm Au layer was performed by the vacuum evaporation method, and the pattern of the metal electrode layer [[3]] was formed by the common lift off method. Then, the wafer was subjected to 400°C, five minute annealing in an N_2 atmosphere, followed by forming 300 nm Si_3N_4 on the entire surface of the wafer as the passivation [[4]] using the plasma CVD. On the Si_3N_4 layer, a resist pattern was formed having openings at the pad portions. Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, followed by removing the resist finally.

Please amend the paragraph at page 76, line 3 to line 17, as follows:

Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the passivation using plasma CVD (S607). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S608). Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S609). Subsequently, the resist was removed (S610), followed by continuous evaporation of the 100 nm Ti layer and 600 nm Au layer by the vacuum evaporation method, and the pattern of the metal electrode layer [[13]] was formed by the common lift off method (S611 and S612). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 79, line 4 to line 13, as follows:

The layer structure and fabrication process of the semiconductor thin film [[2]] were the same as those of the example 13. The wafer process will be described with reference to the flowchart illustrated in Fig. 2. First, a resist pattern (including electrode contact portions) with a shape of the magneto-sensitive pattern was formed by the photolithography (S201). Using it as a mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate by ion milling (S202), followed by removing the resist (S203).

Please amend the paragraph at page 79, line 14 to line 20, as follows:

Subsequently, a resist pattern for exposing the InAs layer [[2b]] was formed using the photolithography (S204). Etching of unnecessary portions of the $GaAs_{0.02}Sb_{0.98}$ layer [[2d]] and $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[2c]] was performed with HCl based etchant (S205), followed by removing the resist (S206). Since the etchant did not etch the InAs layer, the etching stopped on the surface of the InAs layer.

Please amend the paragraph at page 79, line 21, to page 80, line 6, as follows:

Subsequently, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[3]] was formed by the common lift off method (S207). After that, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the passivation [[4]] using plasma CVD (S208). On the Si_3N_4 layer, a resist pattern was formed having openings at the pad portions (S209). Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S210). After removing the

resist, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 81, line 1 to line 10, as follows:

The layer structure and fabrication process of the semiconductor thin film were the same as those of the example 13. The wafer process will be described with reference to the flowchart illustrated in Fig. 20. First, a resist pattern (including electrode contact portions) with a shape of the magneto-sensitive pattern was formed (S2001). Using it as a mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[21]] by ion milling (S2002), followed by removing the resist (S2003).

Please amend the paragraph at page 81, line 20, to page 82, line 3, as follows:

Then, unnecessary portions of the $GaAs_{0.02}Sb_{0.98}$ layer [[22d]] and $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer were etched with HCl based etchant (S2008) to expose the surface of the InAs layer that makes contact with the metal electrode layer. In addition, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[23]] was formed by the common lift off method (S2009 and S2010). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 82, line 25, to page 83, line 13, as follows:

First, the fabrication process of the semiconductor thin films will be described. The semiconductor thin films were formed by successively forming the following compound semiconductor layers on the GaAs substrate two inches in diameter by the

molecular beam epitaxy (MBE): 500 nm $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ as the first compound semiconductor layer; 50 nm InAs as the active layer; 50 nm $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ as the second compound semiconductor layer; and 10 nm GaAs as the third compound semiconductor layer. The band gap of $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ is about 1.2 eV, which is sufficiently greater than 0.36 eV of InAs. The electric characteristics of the semiconductor thin films [[2]] were measured using the van der Pauw method. The results were: the electron mobility was 22000 cm^2/Vs, the sheet resistance was 380 Ω, and the sheet electron concentration was 7.5×10^{11} cm^{-2}.

Please amend the paragraph at page 87, line 26, to page 88, line 12, as follows:

Subsequently, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[47]] using the plasma CVD (S704). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed. Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2. Subsequently, a hard mask was formed by removing the resist (S706). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[41]] by ion milling (S707 and S708). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 88, line 13 to line 21, as follows:

Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[48]] using plasma CVD (S709). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes

contact with the InAs layer and at the pad portions (S710). Then, unnecessary portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S711), followed by removing the resist (S712).

Please amend the paragraph at page 88, line 22, to page 89, line 1, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[33]] was formed by the common lift off method (S713 and S714). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 89, line 25, to page 90, line 9, as follows:

The fabrication process of the semiconductor thin films is the same as that of the example 14. The wafer process was performed based on the flowchart of Fig. 7. First, a resist pattern having openings slightly greater than the regions at which the metal electrode layer makes contact with the InAs layer [[43]] was formed on the semiconductor thin films (S701). Then, unnecessary portions of the GaAs layer [[45]] and part of the $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[44]] were etched by the ion milling, and the residual $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer 44 was etched by the HCl based etchant to expose the InAs surface making contact with the metal electrode layer (S702 and S703).

Please amend the paragraph at page 90, line 10 to line 23, as follows:

Subsequently, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[47]] using the plasma CVD (S704). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed (S705). Then, unnecessary portions of the SiO_2 layer were etched by the

reactive ion etching using the mixed gas of CF_4 and O_2. Subsequently, a hard mask was formed by removing the resist (S706). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[41]] by ion milling (S707 and S708). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 90, line 24, to page 91, line 5, as follows:

Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[48]] using plasma CVD (S709). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S710). Then, unnecessary portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S711), followed by removing the resist (S712).

Please amend the paragraph at page 91, line 6 to line 12, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[33]] was formed by the common lift off method (S713 and S714). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 92, line 9, to line 25, as follows:

The fabrication process of the semiconductor thin films is the same as that of the example 13. The wafer process was performed based on the flowchart of Fig. 9. First, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[57]]

using the plasma CVD (S901). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed (S902). Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, and a hard mask was formed by removing the resist (S903). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[51]] by ion milling (S904 and S905). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 92, line 26, to page 93, line 11, as follows:

Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[58]] using plasma CVD (S906). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S907). Then, unnecessary portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S908), followed by removing the resist (S909). Then, unnecessary portions of the $GaAs_{0.02}Sb_{0.98}$ layer [[42d]] and $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[42c]] were etched by the HCl based etchant to expose the InAs surface making contact with the metal electrode layer (S910).

Please amend the paragraph at page 93, line 12 to line 18, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[56]] was formed by the common lift off method (S911 and S912). Finally, the

wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 94, line 15, to page 95, line 4, as follows:

The fabrication process of the semiconductor thin films is the same as that of the example 13. The wafer process was performed based on the flowchart of Fig. 11. First, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[67]] using the plasma CVD (S1101). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed (S1102). Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, and a hard mask was formed by removing the resist (S1103). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[51]] by ion milling (S1104 and S1105). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 95, line 5 to line 15, as follows:

Subsequently, a resist pattern having openings slightly greater than the regions at which the metal electrode layer makes contact with the InAs layer was formed on the SiO_2 layer (S1106). Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S1107), followed by removing the resist (S1108). After that, unnecessary portions of the $GaAs_{0.02}Sb_{0.98}$ layer [[52d]] and $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[52c]] were etched by the HCl based etchant to expose the InAs surface making contact with the metal electrode layer (S1109).

Please amend the paragraph at page 95, line 16 to line 24, as follows:

Subsequently, 300 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[67]] using plasma CVD (S1110). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S1111). Then, unnecessary portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S1112), followed by removing the resist (S1113).

Please amend the paragraph at page 95, line 25, to page 96, line 4, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[53]] was formed by the common lift off method (S1114 and S1115). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 97, line 1 to line 17, as follows:

The fabrication process of the semiconductor thin films is the same as that of the example 13. The wafer process was performed based on the flowchart of Fig. 12. First, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[77]] using the plasma CVD (S1201). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed (S1202). Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, and a hard mask was formed by removing the resist (S1203). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[61]] by ion milling (S1204

and S1205). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 97, line 18, to page 98, line 3, as follows:

Subsequently, 100 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[78]] using plasma CVD (S1206). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S1207). Then, unnecessary portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S1208), followed by removing the resist (S1209). Then, unnecessary portions of the $GaAs_{0.02}Sb_{0.98}$ layer [[75]] and $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[74]] were etched by the HCl based etchant to expose the InAs surface making contact with the metal electrode layer (S1210).

Please amend the paragraph at page 98, line 4 to line 12, as follows:

Subsequently, 200 nm Si_3N_4 was formed on the entire surface of the wafer as the third passivation [[79]] using plasma CVD (S1211). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S1212). Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, followed by removing the resist (S1213).

Please amend the paragraph at page 98, line 13 to line 19, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[63]] was formed by the common lift off method (S1214 and S1215). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.

Please amend the paragraph at page 99, line 16, to page 100, line 5, as follows:

The fabrication process of the semiconductor thin films is the same as that of the example 14. The wafer process was performed based on the flowchart of Fig. 12. First, a 500 nm SiO_2 was formed on the entire surface of a wafer as the first passivation [[77]] using the plasma CVD (S1201). Subsequently, a resist pattern with a shape of the magneto-sensitive pattern (including electrode contact portions) was formed (S1202). Then, unnecessary portions of the SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2, and a hard mask was formed by removing the resist (S1203). Using the hard mask, the magneto-sensitive pattern was formed by performing the mesa etching down to the GaAs substrate [[71]] by ion milling (S1204 and S1205). During the etching of the semiconductor thin films by the ion milling, the SiO_2 layer of the hard mask was also etched, leaving a film with a thickness of about 100 nm.

Please amend the paragraph at page 100, line 6 to line 19, as follows:

Subsequently, 100 nm Si_3N_4 was formed on the entire surface of the wafer as the second passivation [[78]] using plasma CVD (S1206). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S1207). Then, unnecessary

portions of the Si_3N_4 layer and SiO_2 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S1208), followed by removing the resist (S1209). Subsequently, unnecessary portions of the GaAs layer [[75]] and part of the $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[74]] were etched by the ion milling, and the residual $Al_{0.57}Ga_{0.43}As_{0.04}Sb_{0.96}$ layer [[74]] was etched by the HCl based etchant to expose the InAs surface making contact with the metal electrode layer (S1210).

Please amend the paragraph at page 100, line 20, to page 101, line 1, as follows:

Subsequently, 200 nm Si_3N_4 was formed on the entire surface of the wafer as the third passivation [[79]] using plasma CVD (S1211). On the Si_3N_4 layer, a resist pattern was formed having openings at the regions where the metal electrode layer makes contact with the InAs layer and at the pad portions (S1212). Then, unnecessary portions of the Si_3N_4 layer were etched by the reactive ion etching using the mixed gas of CF_4 and O_2 (S1213), followed by removing the resist.

Please amend the paragraph at page 101, line 2 to line 8, as follows:

Furthermore, the 100 nm Ti layer and 600 nm Au layer were continuously evaporated by the vacuum evaporation method, and the pattern of the metal electrode layer [[63]] was formed by the common lift off method (S1214 and S1215). Finally, the wafer was subjected to 250°C, two hour annealing in an Ar atmosphere, thereby fabricating the compound semiconductor Hall devices.